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INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 7 : H01L

A2

(11) International Publication Number: **WO 00/49643**

(43) International Publication Date: 24 August 2000 (24.08.00)

(21) International Application Number: PCT/US00/03758

(22) International Filing Date: 14 February 2000 (14.02.00)

(30) Priority Data:
09/250,590 16 February 1999 (16.02.99) US

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(81) Designated States: AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CU, CZ, DE, DK, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, UA, UG, UZ, VN, YU, ZW, ARIPO patent (GH, GM, KE, LS, MW, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).

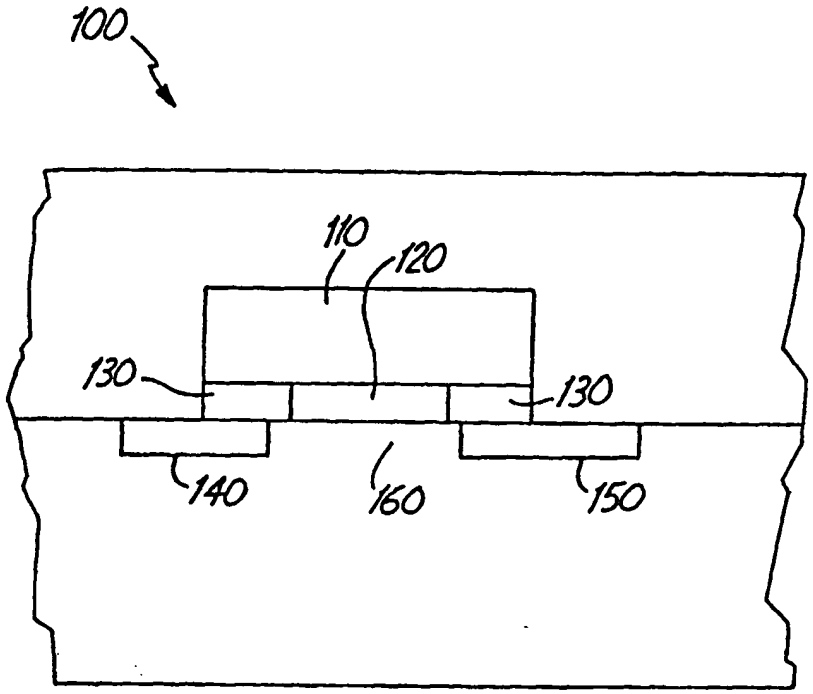
Published

Without international search report and to be republished upon receipt of that report.

(54) Title: SEMICONDUCTOR ARRANGEMENT WITH TRANSISTOR GATE INSULATOR

(57) Abstract

According to one example embodiment, the present invention is directed to a semiconductor device, wherein the device includes a transistor having source and drain regions separated by a channel region. The device includes a gate formed over the channel region and formed over part of the source region and over part of the drain region. The device further includes an insulator region configured and arranged to insulate the gate from the channel region and from the source and drain regions. The insulator region has a first material arranged over the channel region and providing a high dielectric constant, and has a second material arranged over part of the source region and over part of the drain region and providing a significantly lower dielectric constant. By using insulator materials having different dielectric constants, this embodiment not only meets the compact size requirements of higher–functioning devices, but also adequately insulates the gate and channel regions and improves the transistor performance.



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SEMICONDUCTOR ARRANGEMENT WITH TRANSISTOR GATE INSULATOR

Field of the Invention

The present invention relates generally to semiconductor devices and their fabrication and, more particularly, to semiconductor devices and their manufacture involving dielectrics used with transistors.

Background of the Invention

The electronics industry continues to rely upon advances in semiconductor technology to realize higher-functioning devices in more compact areas. For many applications, realizing higher-functioning devices requires integrating a large number of electronic devices into a single silicon wafer. In addition, many of the individual devices within the wafer are being manufactured with smaller physical dimensions. As the number of electronic devices per given area of the silicon wafer increases, and as the size of the individual devices decreases, the manufacturing process becomes difficult.

A large variety of semiconductor devices have been manufactured having various applications in numerous disciplines. Such silicon-based semiconductor devices often include metal-oxide-semiconductor (MOS) transistors, such as p-channel MOS (PMOS), n-channel MOS (NMOS), complementary MOS (CMOS), bipolar complementary MOS (BiCMOS), and bipolar transistors.

Each of these semiconductor devices generally includes a semiconductor substrate on which a number of active devices are formed. The particular structure of a given active device can vary between device types. For example, in MOS transistors, an active device generally includes source and drain regions and a gate electrode which modulates current between the source and drain regions.

As devices are scaled below 0.18 microns, gate insulator thicknesses reach the quantum mechanical regime. One gate insulator material used in this regime is silicon dioxide. Current research indicates that silicon dioxide thicknesses of 20-25 angstroms will result in unacceptably large tunneling currents. To alleviate this problem, research has begun on alternatives to silicon dioxide that have larger dielectric constants. This

allows the use of thicker gate insulators, diminishing the gate tunneling current without reducing the gate capacitance. However, large capacitance is not desirable in the source-drain overlap regions of the gate because it increases the gate to source-drain, or overlap, capacitance and degrades transistor performance. The gate-to-drain capacitance is particularly critical for transistor performance as it is amplified during switching due to the Miller effect.

Previous work on this problem has mostly focused on thickening the gate oxide over the source-drain region to reduce overlap capacitance. This provides only a modest reduction in overlap capacitance and creates stress in the gate.

With the demands for increasing the density of such MOS-based circuits continuing to escalate, there is an ongoing need to reduce the amount of real estate consumed by various aspects of the circuits and to minimize the complexities and deficiencies resulting from manufacturing processes.

Summary of the Invention

The present invention is directed to a transistor gate insulator material that not only meets the compact size requirements of higher-functioning devices but also adequately insulates the gate and channel regions and improves the transistor performance. The present invention is exemplified in a number of implementations and applications, some of which are summarized below.

According to an example embodiment, the present invention is directed to a semiconductor device that includes a transistor comprising source and drain regions separated by a channel region. A gate is formed over the channel region, over part of the source region, and over part of the drain region. An insulator region is configured and arranged to insulate the gate from the channel region and from the source and drain regions. The insulator region has a first material arranged substantially over the channel region and providing a high dielectric constant, and a second material arranged substantially over part of the source region and over part of the drain region and providing a significantly lower dielectric constant.

In another example embodiment, the present invention is directed to a method for manufacturing a semiconductor device. The device includes source and drain regions separated by a channel region, and an insulator region. The insulator region is

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Each of these semiconductor devices generally includes a semiconductor substrate on which a number of active devices are formed. The particular structure of a given active device can vary between device types. For example, in MOS transistors, an active device generally includes source and drain regions and a gate electrode which modulates current between the source and drain regions.

As devices are scaled below 0.18 microns, gate insulator thicknesses reach the quantum mechanical regime. One gate insulator material used in this regime is silicon dioxide. Current research indicates that silicon dioxide thicknesses of 20-25 angstroms will result in unacceptably large tunneling currents. To alleviate this problem, research has begun on alternatives to silicon dioxide that have larger dielectric constants. This

over-etched to form recesses at corners of the gate adjacent the source and drain regions. A second material is formed in the recesses.

In yet another example embodiment, a semiconductor device that includes a transistor having source and drain regions separated by a channel region is provided. A gate is formed over the channel region, over part of the source region, and over part of the drain region. An insulator region is configured and arranged to insulate the gate from the channel region and from the source and drain regions. The insulator region has means, arranged over the channel region, for providing a high dielectric constant. The insulator region also has means, arranged over the part of the source region and over the part of the drain region, for providing a significantly lower dielectric constant.

The above summary of the present invention is not intended to describe each illustrated embodiment or every implementation of the present invention. The figures and detailed description which follow more particularly exemplify these embodiments.

Brief Description of the Drawings

The invention may be more completely understood in consideration of the following detailed description in connection with the accompanying drawings, in which:

FIG. 1 is a cross-sectional view of a semiconductor device with an insulator region adjacent to source, drain, channel, and gate regions, according to an example embodiment of the present invention;

FIG. 2 is a cross-sectional view of a semiconductor device with source, drain, and channel regions, a first insulator layer having a high dielectric constant, and a gate region formed over the insulator layer, according to another example embodiment of the present invention;

FIG. 3 is a cross-sectional view of a semiconductor device wherein part of a first insulator layer having a high dielectric constant has been removed, according to another example embodiment of the present invention;

FIG. 4 is a cross-sectional view of a semiconductor device with a second insulator layer having a low dielectric constant, according to yet another example embodiment of the present invention; and

FIG. 5 is a cross-sectional view of a semiconductor device wherein part of a second insulator layer having a low dielectric constant has been removed, according to still another example embodiment of the present invention.

While the invention is amenable to various modifications and alternative forms, certain specifics thereof have been shown by way of example in the drawings and will be described in detail. It should be understood, however, that the intention is not to limit the invention to the particular embodiments described. On the contrary, the intention is to cover all modifications, equivalents, and alternatives falling within the spirit and scope of the invention as defined by the appended claims.

Detailed Description

The present invention is directed to using decreased gate insulator thicknesses while maintaining or improving transistor performance; and applicable, for example, where gate insulator thicknesses are reduced to 20-25 angstroms and where unacceptable large tunneling currents occur. The present invention has been found to be particularly advantageous for use in applications requiring small insulator thicknesses when using a combination of insulator materials such as silicon nitride, silicon dioxide, tantalum oxide, or fluorine-doped silicon oxide (SiOF). While the present invention is not necessarily limited to these materials, an appreciation of various aspects of the invention may be appreciated through a discussion of one or more examples using this context.

According to an example embodiment, the present invention is directed to a semiconductor device that has source and drain regions separated by a channel region. A gate is located over the channel region, over part of the source region, and over part of the drain region. An insulator region is positioned between the gate and the source, drain, and channel regions. The insulator region has a first material having a high dielectric constant arranged substantially over the channel region, and a second material having a low dielectric constant arranged substantially over part of the source region and part of the drain region. A notable advantage of this arrangement is that, in using an insulator layer comprising a combination of materials with different dielectric constants, the gate to channel capacitance remains high, reducing tunneling currents, and the overlap capacitance is reduced, improving the transistor performance.

The insulator material may be arranged with certain portions of the first or second material over respective portions of the source, drain, and channel regions. For instance, the first material may be arranged to overlap both the channel, source, and drain regions. The first material may also be arranged to overlap only the channel region. In addition, the second material may be arranged to overlap only the source and drain regions. The second material may also be arranged to overlap the channel, source, and drain regions.

FIG. 1 shows a transistor device 100, according to another example embodiment of the present invention. A gate 110 is arranged over source 140, drain 150, and channel 160 regions. Insulator layer 120 is located between the gate 110 and channel 160 region. An insulator layer 130 is located between the gate 110 and source 140 and channel 160 regions. Another insulator layer 130 is located between the gate 110 and drain 150 and channel 160 regions. The insulator layer 120 includes material having a high dielectric constant of between about 6 and about 25. The material in insulator layer 120 may include, for example, silicon nitride or tantalum oxide. The insulator layers 130 include material having a low dielectric constant of between about 2.5 and about 4. The material in insulator layers 130 may include, for example, silicon dioxide or SiOF.

In another example embodiment, the present invention includes a method for manufacturing a semiconductor device having source and drain regions separated by a channel region, and having an insulator region, as shown, for example, in FIGs. 2 - 5. FIG. 2 shows a cut-away view of a semiconductor device having a source region 230, a drain region 240, and a channel region 250. A first insulator layer 220 having a high dielectric constant is formed over the source, drain, and channel regions. A gate 210 is formed over the first insulator layer 220 and over the source 230, drain240. and channel 250 regions. FIG. 3 shows another cut-away view wherein the first insulator layer 220 is over-etched to form recess areas 310 and 320 at corners of the gate 210 adjacent the source 230 and drain 240 regions. The recess areas may be formed using, for example, wet-etching, as used in manufacturing for isolation technologies such as poly-encapsulated local oxidation (PELOX). In an example PELOX process, isotropic etching is used to create a recess area by removing unprotected portions of a layer below a surface layer, resulting in lateral undercut of the layer below the surface area.

FIG. 4 shows yet another cut-away view wherein a second insulator layer 410 is formed over the source 230, drain 240, and gate 210 regions, and extends into the recess areas as shown in FIG. 3. The second insulator layer 410 may be formed, for example, by deposition or growth in the recess areas. FIG. 5 shows another cut-away view wherein the second insulator layer 410 is partially removed, leaving only that much material which about occupies the recess areas under the gate 210.

While the present invention has been described with reference to several particular example embodiments, those skilled in the art will recognize that many changes may be made thereto without departing from the spirit and scope of the present invention, which is set forth in the following claims.

What is claimed is:

1. A semiconductor device, comprising:

a transistor having source and drain regions (140, 150) separated by a channel region (160), having a gate (110) formed over the channel region and formed over part of the source region and over part of the drain region, and an insulator region (130) configured and arranged to insulate the gate from the channel region and from the source and drain regions; and

the insulator region having a first material (120) arranged over the channel region to provide a high dielectric constant, and having a second material (130) arranged over the part of the source region and over the part of the drain region to provide a significantly lower dielectric constant.

2. A semiconductor device, according to claim 1, wherein the second material is not arranged to overlap the channel region.

3. A semiconductor device, according to claim 1, wherein the first material is further arranged to overlap respective portions of the source and drain regions.

4. A semiconductor device, according to claim 1, wherein the second material is fluorine-doped silicon oxide.

5. A semiconductor device, according to claim 1, wherein the second material includes silicon dioxide.

6. A semiconductor device, according to claim 1, wherein the first material is silicon nitride.

7. A semiconductor device, according to claim 1, wherein the first material includes tantalum oxide.

8. A semiconductor device, according to claim 1, wherein the second material is configured and arranged to provide overlap capacitance that is reduced relative to the first material being used.

9. A semiconductor device, according to claim 1, wherein the first material includes nitride and the second material includes oxide.

10. A semiconductor device, according to claim 1, wherein the first insulator material includes material with a dielectric constant of between about 6 and about 25.

11. A semiconductor device, according to claim 1, wherein the gate forms corners adjacent the source and drain regions.

12. A semiconductor device, comprising:

a transistor having source and drain regions separated by a channel region, having a gate formed over the channel region and formed over part of the source region and over part of the drain region, and an insulator region configured and arranged to insulate the gate from the channel region and from the source and drain regions; and

the insulator region having means, arranged substantially over the channel region, for providing a high dielectric constant, and having means, arranged substantially over the source region and substantially over the drain region, for providing a low dielectric constant.

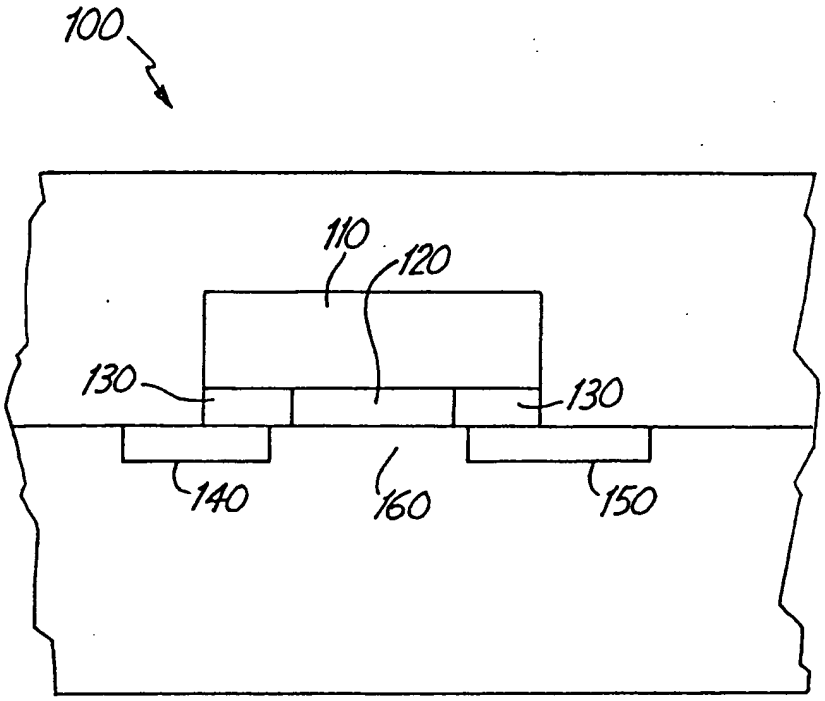

FIG. 1

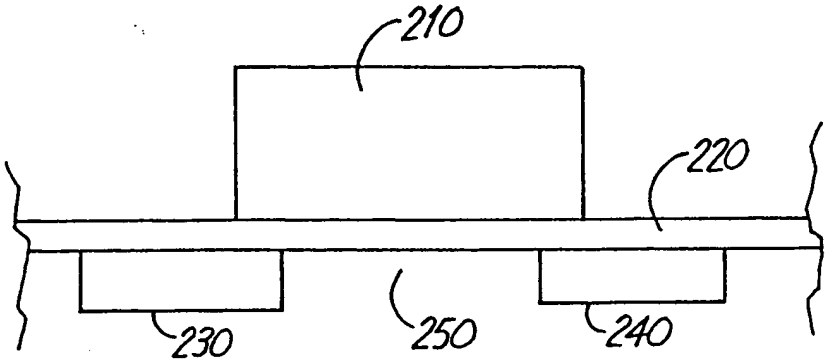

FIG. 2

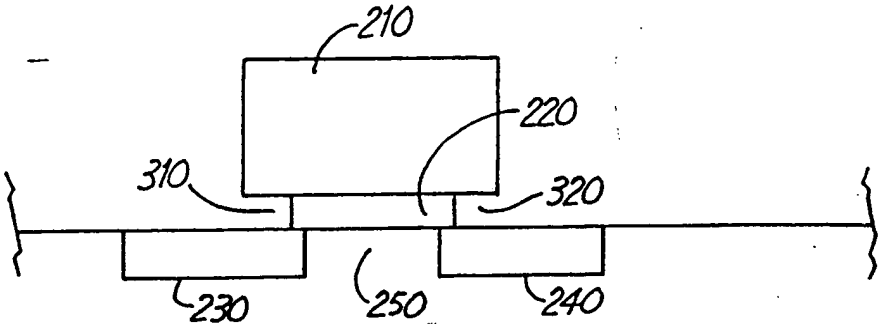

FIG. 3

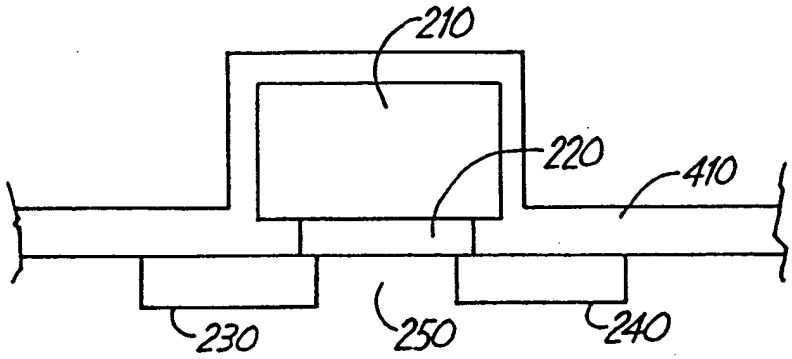

FIG. 4

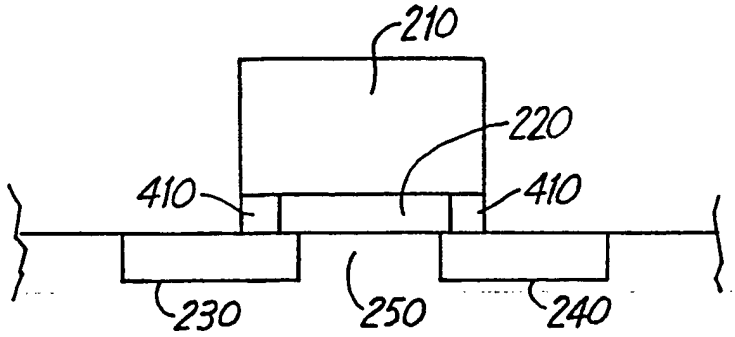

FIG. 5

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
24 August 2000 (24.08.2000)

PCT

(10) International Publication Number
WO 00/49643 A3

(51) International Patent Classification[7]: H01L 29/51

(21) International Application Number: PCT/US00/03758

(22) International Filing Date: 14 February 2000 (14.02.2000)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
09/250,590 16 February 1999 (16.02.1999) US

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(74) Agent: CRAWFORD, Robert, J.; Crawford PLLC, Suite 390, 1270 Northland Drive, SAINT PAUL, MN 55120 (US).

(81) Designated States *(national)*: AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CU, CZ, DE, DK, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, UA, UG, UZ, VN, YU, ZW.

(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).

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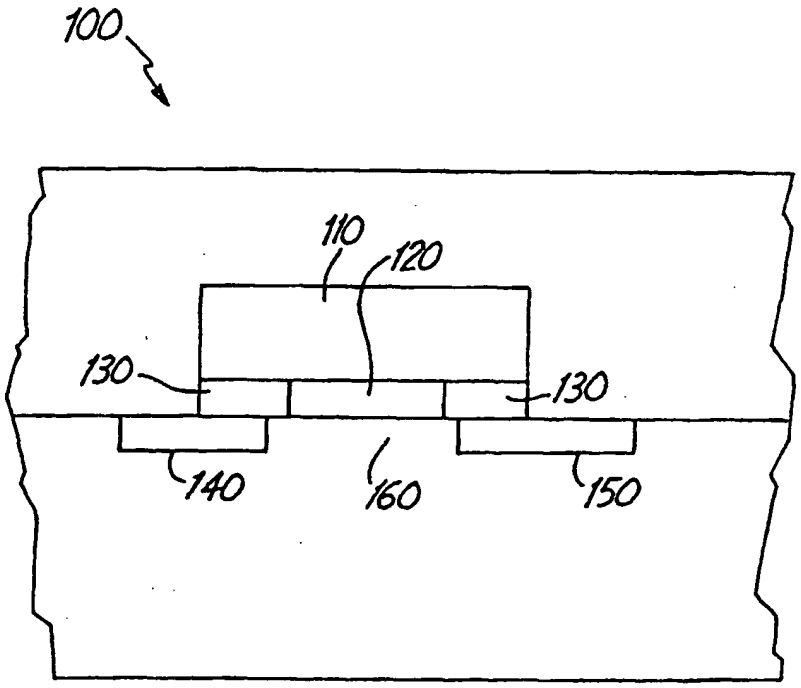
(54) Title: GATE INSULATOR COMPRISING HIGH AND LOW DIELECTRIC CONSTANT PARTS



(57) Abstract: According to one example embodiment, the present invention is directed to a semiconductor device, wherein the device includes a transistor having source and drain regions separated by a channel region. The device includes a gate formed over the channel region and formed over part of the source region and over part of the drain region. The device further includes an insulator region configured and arranged to insulate the gate from the channel region and from the source and drain regions. The insulator region has

[Continued on next page]

WO 00/49643 A3

Published:
— *With international search report.*
— *Before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments.*

(88) Date of publication of the international search report:
15 February 2001

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a first material arranged over the channel region and providing a high dielectric constant, and has a second material arranged over part of the source region and over part of the drain region and providing a significantly lower dielectric constant. By using insulator materials having different dielectric constants, this embodiment not only meets the compact size requirements of higher-functioning devices, but also adequately insulates the gate and channel regions and improves the transistor performance.

INTERNATIONAL SEARCH REPORT

Intern· nal Application No
PCT/US 00/03758

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L29/51

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

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C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	PATENT ABSTRACTS OF JAPAN vol. 1999, no. 04, 30 April 1999 (1999-04-30) -& JP 11 003990 A (SONY CORP), 6 January 1999 (1999-01-06) abstract paragraphs '0016!-'0032!; figure 1 paragraphs '0053!-'0057!; figure 11 paragraphs '0061!-'0092!; figures 13-17 paragraphs '0047!,'0048!; figure 9	1-12
X	PATENT ABSTRACTS OF JAPAN vol. 015, no. 098 (E-1042), 8 March 1991 (1991-03-08) -& JP 02 307271 A (MITSUBISHI ELECTRIC CORP), 20 December 1990 (1990-12-20) abstract; figures 1-4	1-3,5,6, 8-12

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[ ] Patent family members are listed in annex.

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Name and mailing address of the ISA	Authorized officer
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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

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X	PATENT ABSTRACTS OF JAPAN vol. 007, no. 178 (E-191), 6 August 1983 (1983-08-06) -& JP 58 084462 A (TOKYO SHIBAURA DENKI KK), 20 May 1983 (1983-05-20) abstract; figures 1-3	1,3,5,6, 8-12

INTERNATIONAL SEARCH REPORT

Information on patent family members

Inter nal Application No
PCT/US 00/03758

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
JP 11003990 A	06-01-1999	NONE	
JP 02307271 A	20-12-1990	NONE	
JP 58084462 A	20-05-1983	NONE	